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Design of High Performance Quaternary Adders

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***Abstract*—Design of the binary logic circuits is limited by the requirement of the interconnections. A possible solution could be arrived at by using a larger set of signals over the same chip area. Multiple-valued logic (MVL) designs are gaining importance from that perspective. This paper presents the design of a multiple-valued half adder and full adder circuits. The proposed adders are implemented in Multiple-Valued voltage-Mode Logic (MV-VM*L*). In quaternary half adder, quaternary logic levels are first converted to binary and binary logic levels are used for the purpose of addition. Addition operation is performed with less number of gates and minimum depth of net. A full adder circuit is designed by converting the quaternary logic in to unique code, which enables to implement circuit with reduced hard ware. Sum and carry are processed in two separate blocks, controlled by code generator unit. Simple pass transistors are used for implementation. The design is targeted for the 0.18 µm CMOS technology and verification of the design is done through HSPICE and COSMOSCOPE Synopsis Tools. Area of the designed circuits is less than the corresponding binary circuits and quaternary adders because number of transistors used are less. Intensive simulation on Hspice also shows high performance of the proposed circuits.**

***Index Terms*—Down literal circuit, multi-level logic, quaternary full adder, quaternary half adder.**

I. Introduction

Increased data density, reduced dynamic power dissipation, and increased computational ability are among some of the key benefits of Multiple Valued Logic (MVL). Several implementation methods have been proposed in the recent papers to realize the MVL circuits [1, 2]. They can fundamentally be categorized as current-mode, voltage-mode and mixed-mode circuits. Several prototype chips of current-mode CMOS circuits have been fabricated, showing somewhat better performances compared to the corresponding binary circuits [3-6]. Even though current-mode circuits have been popular and offer several benefits, the power consumption is high due to their inherent nature of constant current flow during the operation. Alternatively, voltage-mode circuits consume a large majority of power only during the logic level switching. Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. Several approaches for quaternary circuit design have been proposed [7-12], in voltage mode technique.

Quaternary logic (radix-4-valued) is chosen as the base radix for the work reported here. Using a quaternary radix offers all the benefits of MVL such as reduced area due to signal routing reduction along with the important advantage of being able to easily interface with traditional binary logic circuits.

The organization of the paper is as follows: Section 2 explains discussion of previous research related to the proposed work. Implementation of quaternary half adder is shown in section 3. In section 4, quaternary full adder circuit is explained along with simulation results. Conclusion part of the paper is given in section 5.

A. Review of MVL adder designs

Novel quaternary half adder, full adder, and a carry-look ahead adder were introduced by M Thoidis [13]. In his paper, the proposed circuits were static and operate in voltage mode. They reported no static power dissipation as the circuits were static in nature.

Ricardo designed a new truly full adder quaternary circuit using 3 power supply lines and multi-V_t transistors. He has designed quaternary multiplexer (MUX) 4:1 with 4 quaternary inputs and one quaternary output and used this MUX as a building block to construct full adder. Proposed technique benefits large scale circuits since the much power dissipation with increased speed can lead to the development of extremely low energy circuits while sustaining the high performance required for many applications [14].

Quaternary full adders based on output generator sharing are proposed by Hirokatsu with reduction in delay and power [15]. The implementation of Quaternary Signed Digit addition was presented in paper [16]. The test confirms the superior performance of the QSD adder implementation over other adders due to the carry - free addition scheme. The complexity of the QSD adder was linearly proportional to the number of digits, which are of the same order as the simplest adder, the ripple carry adder. This QSD adder can be used as a building block for other arithmetic operations such as multiplication, division, square root, etc. With the QSD addition scheme, some well-known arithmetic algorithms can be directly implemented [16].

Supplementary Symmetrical Logic Circuit (referred as SUSLOC) was presented in [17]. This work illustrates how quaternary gates can be implemented using the SUSLOC circuit structure. These gates were then used to build three different addition circuit architectures: carry-ripple, carry-look ahead, and carry-select. These three quaternary addition circuits are then modeled using the System Verilog language. The three different adder

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architectures are designed and compared for area and estimated performance with their binary circuit counterparts [17].

II. Implementation of Quaternary Half Adder

In quaternary logic, addition can be performed in many ways. Numbers in quaternary logic can be directly added or numbers in quaternary logic can be converted to binary logic and addition can be performed in binary logic. Binary results of addition can be displayed in quaternary logic after conversion. Hence quaternary to binary converter is required in the beginning. Binary to quaternary converter is used to display the result in quaternary logic. In [18] modulo-4 addition is introduced, without the hardware for implementation of carry. In this paper proposed half adder has hardware for carry also. Two bit natural representation of binary logic is used for each quaternary number and addition is performed in binary itself with only 4 gates. Figure 1 explains the block diagram of quaternary half adder and table 2 explains the behaviour of this half adder. As shown in table 1, X and Y are quaternary numbers which are converted to 2 bit binary numbers using quaternary to binary converter [19]. X_0, X_1 are the two bit binary representation of X, where as Y_0 and Y_1 are the two bit representation of quaternary number Y. In table 1, S_1 and S_0 are the result of addition in binary and S is in quaternary because binary to quaternary converter is used for conversion. C_1 and C_0 are in binary. In table 1, carry is nothing but C_0 and actually conversion is not required. Sum generator block shown in figure 1 has 4 binary logic gates as explained in figure 2. Carry generator block is explained in figure 3.

A. Sum Generator Block

Sum generator circuit is shown figure 2. X_0, X_1 are the binary representation of the quaternary number X, and Y_0 and Y_1 are the two bit representation of quaternary number Y. S_0 S_1 are the outputs of sum generator block which is in binary. Minimal functions have been obtained from the Karnaugh diagrams for the tables shown in table 1 and then simplified as much as possible using all possible gate types. Minimal functions obtained from the minimal polynomials extracted from the Karnaugh diagrams are shown below.

$S_0 = x_0 y_0' + x_0' y_0 = (x_0 \oplus y_0)$

$S_1 = (x_1 \oplus y_1) \oplus (x_0 y_0)$

Sum generator in figure 2 is designed using these two expressions. This circuit uses 3 binary XOR gates and one binary AND gate. Depth of net is maximum of two gates. Depth of net is nothing but the number of gates between input and the output.

B. Carry Generator Block

Carry generator circuit is shown figure 3. X_0, X_1 and Y_0 Y_1 are the input to the block. C_o C_1 are the outputs of the block. This circuit is designed by the expression obtained from the Karnaugh diagrams for the tables shown in table 1 and then simplified as much as possible using all possible gate types.

$C_0 = x_1 y_1 + x_0 y_0 (x_1 + y_1)$ and $C_1 = 0$

The circuit contains two binary OR gates and three binary AND gates. Depth of the net is three. Simulation result shown in figure 4 verifies the table 1.

TABLE I: Truth Table of Quaternary Half Adder.

X	Y	X_1	X_0	Y_1	Y_0	S_1	S_0	C_1	C_0	S	C
0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	1	0	1	0	0	1	0
0	2	0	0	1	0	1	0	0	0	2	0
0	3	0	0	1	1	1	1	0	0	3	0
1	0	0	1	0	0	0	1	0	0	1	0
1	1	0	1	0	1	1	0	0	0	2	0
1	2	0	1	1	0	1	1	0	0	3	0
1	3	0	1	1	1	0	0	0	1	0	1
2	0	1	0	0	0	1	0	0	0	2	0
2	1	1	0	0	1	1	1	0	0	3	0
2	2	1	0	1	0	0	0	0	1	0	1
2	3	1	0	1	1	0	1	0	1	1	1
3	0	1	1	0	0	1	1	0	0	3	0
3	1	1	1	0	1	0	0	0	1	0	1
3	2	1	1	1	0	0	1	0	1	1	1
3	3	1	1	1	1	1	0	0	1	2	1

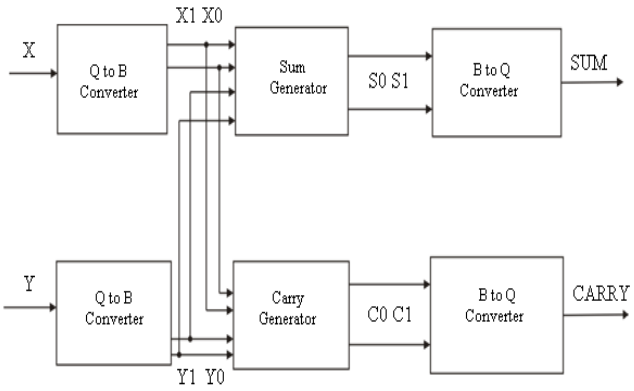

Figure 1: Block diagram of quaternary half adder circuit

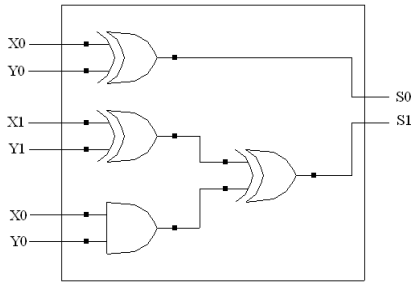

Figure 2: Sum generator circuit

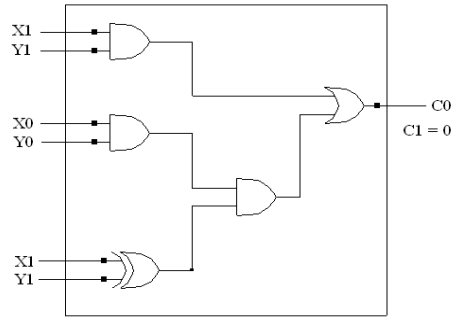

Figure 3:Carry generator circuit

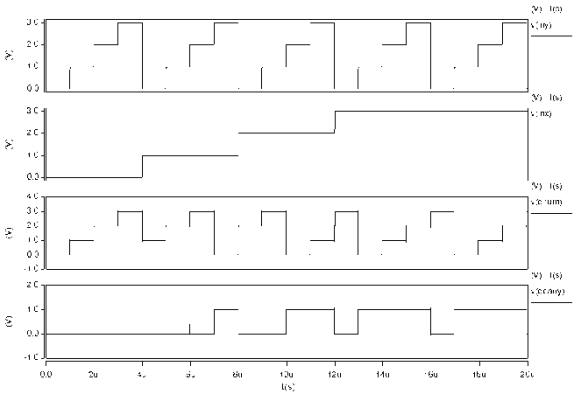

Figure 4: Simulation result of quaternary half adder

A basic Quaternary to binary converter uses three down literal circuits DLC1, DLC2, DLC3 and 2:1 multiplexer. Q is the quaternary input varying as 0, 1, 2 and 3 which is given to three DLC circuits. The binary out puts thus obtained will be in complemented form and are required to pass through inverters to get actual binary numbers.

A basic binary to quaternary circuit consists of two PMOS and two NMOS transistors which form two inverters and two DLC 1 circuits. LSB and MSB of 2 bit binary numbers are given to two DLC1 circuits and output of two inverters will provide quaternary number.

TABLE II: TRUTH TABLE OF QUATERNARY FULL ADDITION WHEN CARRY IN IS 0

Sum

		X			
		0	1	2	3
Y	0	0	1	2	3
	1	1	2	3	0
	2	2	3	0	1
	3	3	0	1	2

Carry

		X			
		0	1	2	3
Y	0	0	0	0	0
	1	0	0	0	1
	2	0	0	1	1
	3	0	1	1	1

TABLE III: TRUTH TABLES OF QUATERNARY FULL ADDITION, WHEN CARRY IN IS 1.

Sum

		X			
		0	1	2	3
Y	0	1	2	3	0
	1	2	3	0	1
	2	3	0	1	2
	3	0	1	2	3

Carry

		X			
		0	1	2	3
Y	0	0	0	0	1
	1	0	0	1	1
	2	0	1	1	1
	3	1	1	1	1

III. IMPLEMENTATION OF QUATERNARY FULL ADDER

Proposed full adder circuit is based on Encoder, code generator, sum block and carry block. Encoder is required for the conversion shown in table 4, consists of DLC1 and DLC3 (Down literal circuit) [18]. Output codes of the Code generator is used to generate sum and carry of the full adder circuit. Block diagram of the full adder circuit is shown in figure 5. Logic levels of quaternary inputs 0, 1, 2 and 3 are represented by the voltage levels of 0V, 1V, 2V and 3V respectively. X and Y are the two quaternary inputs to the full adder. Table 2 shows sum and carry for all possible combinations of inputs when carry input is zero. Table 3 shows sum and carry for all possible combinations of inputs when carry input is one.

TABLE IV: REPRESENTATION OF QUATERNARY TO BINARY CONVERSION

X(Y)	Xp (Yp)	Xq (Yq)
0	0	0
1	1	0
2	1	1
3	0	1

A. Encoder block

Proposed full adder circuit consists of encoder block which converts quaternary numbers X and Y into binary representation as shown in table 4. Output of the encoder is fed to the code generator unit. This block generates codes which are required for the sum and carry block to generate final value of sum and carry. Encoder block consists of down literal circuit 1(DLC1) and Down Literal Circuit 3(DLC 3). Each DLC has two transistors with different threshold voltages and power supply voltages. Down literal circuits along with binary XOR gate is used to give Xp and two quaternary inverters are also used in figure 6 to generate Xq and hence required representation [7]. Yp and Yq are generated in the same way.

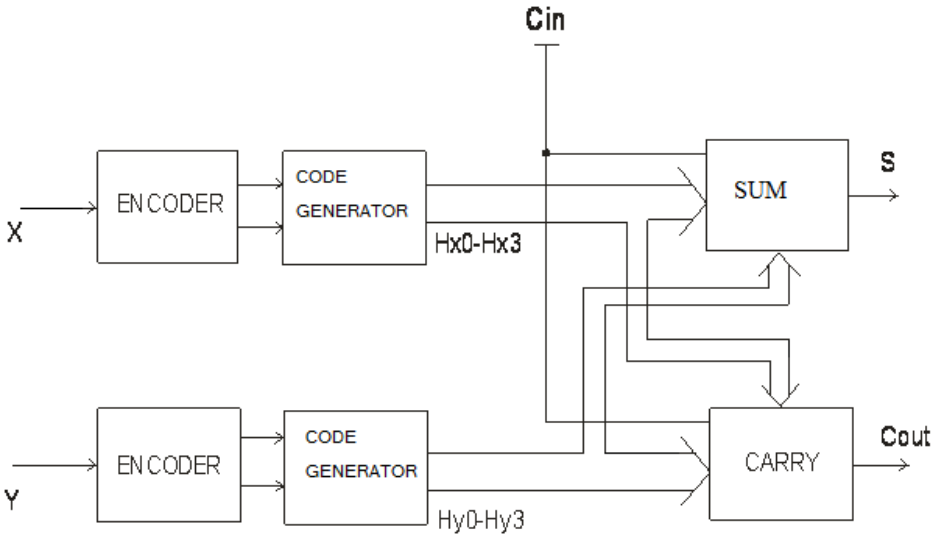

Figure 5: Proposed quaternary full adder

B. *Code generator block*

Block diagram of the Code generator for X and Y is shown in figure 7. As seen in the previous section Quaternary input X is split up in to two equivalent binary numbers Xp and Xq. These two signals are used to generate Hx0, Hx1, Hx2, and Hx3. Quaternary input Y is split up in to two equivalent binary numbers Yp and Yq. These two signals are used to generate Hy0, Hy1, Hy2, and Hy3. Figure 8 shows the circuit diagram of the code generator circuit. It consists of four AND gates

C. *Sum and carry block.*

Sum and carry blocks are built with pass transistors. Quaternary voltage levels are switched towards output according to the levels of the input. The codes generated by the code generator blocks Hx0, Hx1, Hx2, Hx3, Hy0, Hy1, Hy2 and Hy3 are used to control these pass transistors. Circuit diagrams for sum and carry are shown in figure 9 and figure 10 respectively. Figure 11 shows simulation result of addition of two quaternary inputs of the full adder circuit when the carry is zero. Figure 12 verifies the functionality of the circuit when carry is one.

IV. Result and Discussion

The investigation which includes the three quaternary full adder circuits, proposed by Recardo Cuna et.al [14], Hirokatsu Shirahama et.al [15], Hirokatsu Shirahama et.al [20] and corresponding binary adder. In paper [14] 180nm technology file and power supply of 3V is used. It is dissipating dynamic power supply of 181 µW at 250 MHz and it shows delay of 2.24ns. It requires 332 transistors. Paper [15] uses 90nm technology files and 1.2V power supply. Propagation delay of 113ps and dynamic power 55 µW at 1 GHz is observed.. In [20] 180nm and 1.8V power supply is used. Propagation delay of 1.4ns and power dissipation of 194 µW is observed at 300MHz.

We have used 180 nm technology, 3 V power supply and 250 M Hz on synopsys Hspice and Cscope for full adder design and 1GHz for half adder design. Logic levels are well defined and independent of fabrication process variations of the component. The comparisons shown in table 5 summarize the observations of various adder circuits designed in the past**.** In terms of area, we counted the number of transistors required for each of the quaternary and binary equivalent circuits. We realize that the number of transistors used in both the quaternary circuits are less than that of binary equivalent circuit and previously designed quaternary circuits. Area reduction is due to pass transistors and the binary representation used for quaternary logic signals. In terms of performance, we simply found the longest gate path from input to output. The half adder circuit has depth of net as two, where as in full adder; signal has to pass through maximum of three transistors.

Power dissipation and delay are observed for sum and carry blocks of both half adder and full adder. Proposed half adder dissipates 112 µW of power at 1 GHz and shows delay of 1.8 ns. Number of transistors required are 76. Proposed full adder dissipates 84 µW of power at 250 MHz and delay of 2.02 ns and number of transistors required are 148. The use of appropriate input value conversion makes it possible to reduce the hardware.

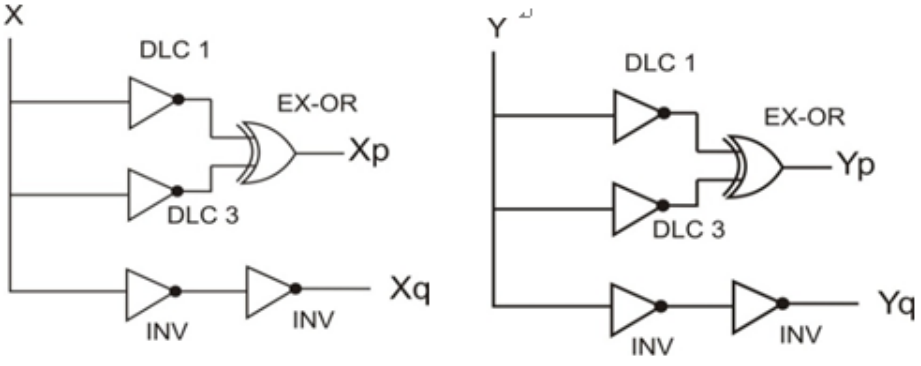

Figure 6: Logic diagrams of encoder circuits.

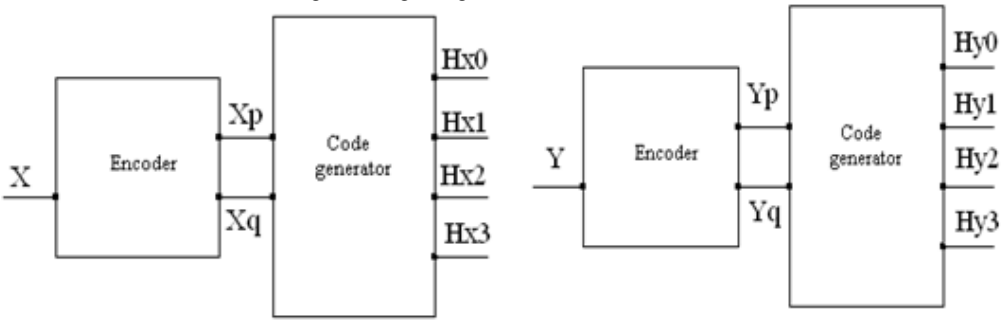

Figure 7: Block diagram of Code generator for quaternary input X and Y.

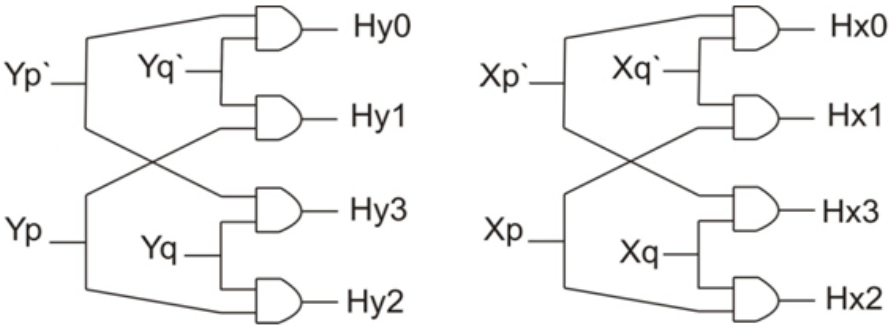

Figure 8: Code generator circuit for quaternary input X and Y

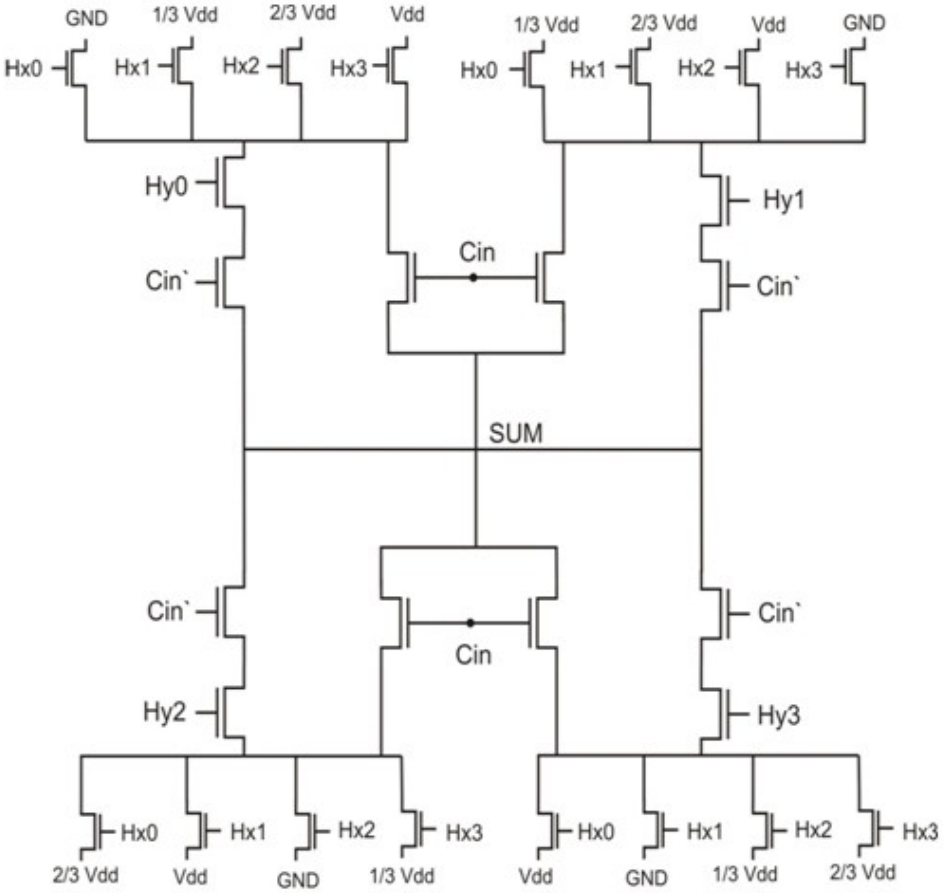

Figure 9: Circuit diagram of Sum block for quaternary full adder

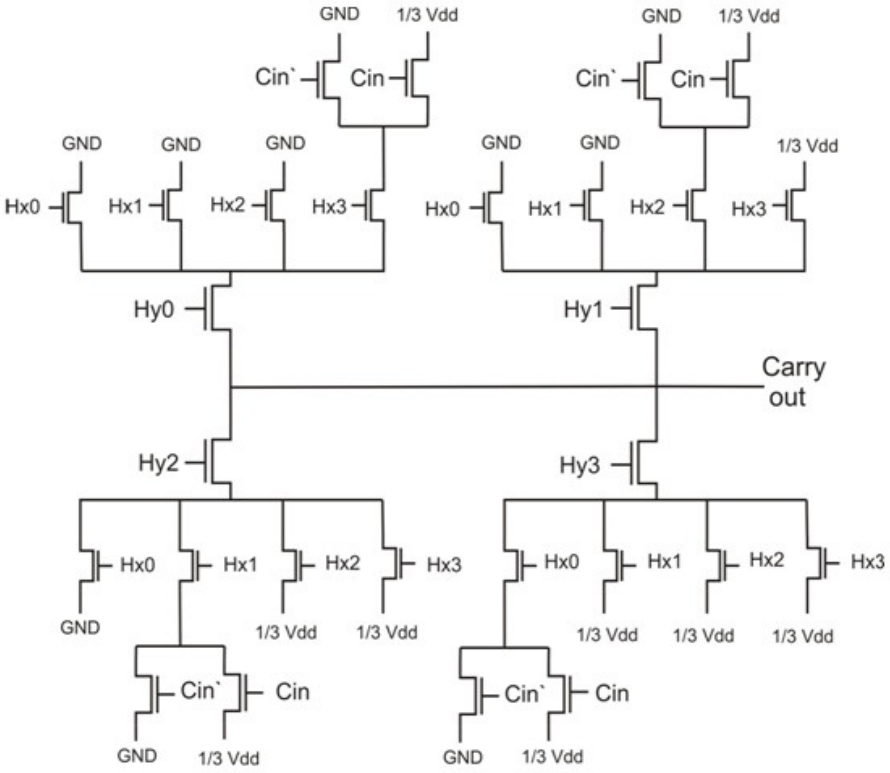

Figure 10: Circuit diagram of carry block for quaternary full adder

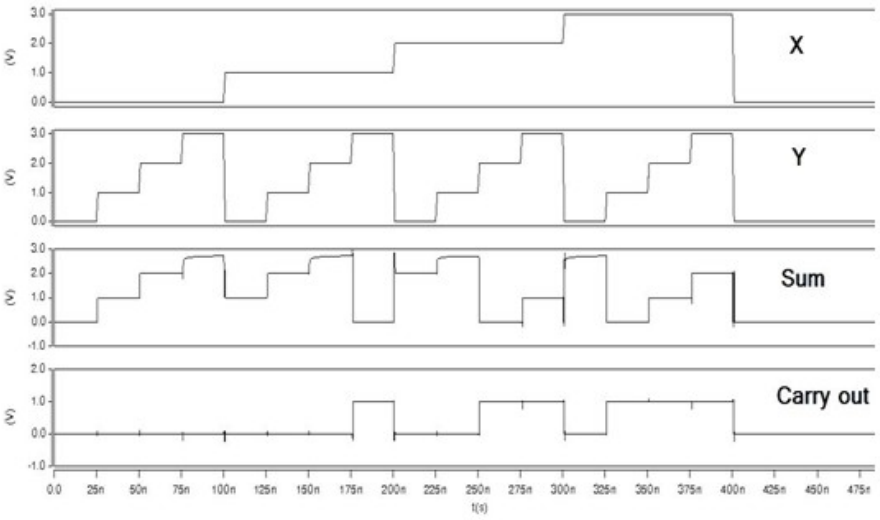

Figure 11: Results of Quaternary Full Adder with Carry 0.

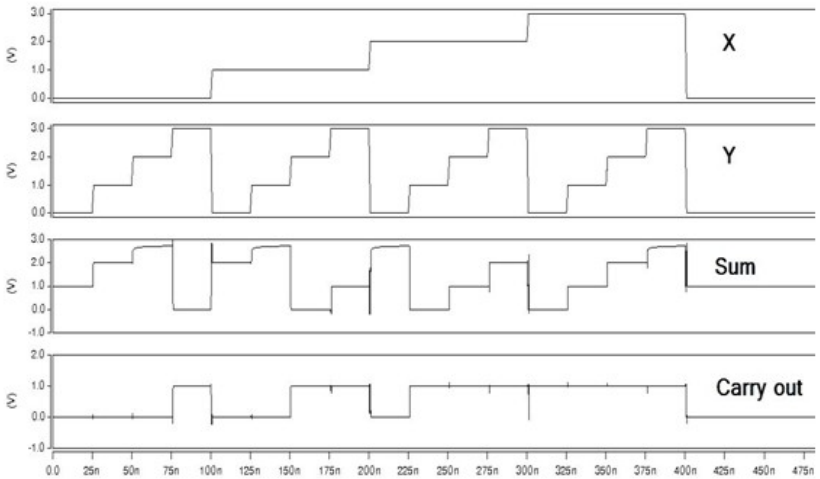

Figure 12: Results of Quaternary Full Adder with Carry 1

V. Conclusion

Quaternary half adders are designed using binary logic gates and radix converters. Quaternary half adder requires only 76 transistors and dissipates 112 µW of power at 1GHz. Quaternary full adder is designed with down literal circuit, code generators, Sum and Carry blocks which requires 148 transistors and dissipates 84µW at 250MHz. Selection of different representation for the quaternary input in binary has reduced the requirement of the more hardware which enables to implement high performance quaternary full adder. Simulation of the proposed circuits is carried out targeted for 180nm technology using HSPICE and COSMOS tools. These circuits consume less number of transistors and shows high performance. Consequently, this design is appropriate to be applied for construction of a high performance multiprocessor which consists of many processing elements.

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TABLE V: Comparison of the performance of the proposed circuits with the works of other authors.

Circuit type	Author	Technology and Max.power supply	Propagation delay	Transistor count	Dynamic power dissipation
Quaternary full adder (Based on Quaternary mux)	Recardo Cuna et.al [14] 2006	180nm, 3V	2.24ns	332	181µW(250MHz)
Equivalent Binary adder		180nm, 3V	2.66ns	276	762µW(250MHz)
Quaternary full adder (Based on Output generator sharing)	Hirokatsu Shirahama et.al[15] 2008	90nm,1.2V	113ps	252	55 µW(1G Hz)

Quaternary full adder (Based on Quaternary Differential logic)	Hirokatsu Shirahama et.al[20] 2007	180nm,1.8V	1.4ns	194	194 µW(300MHz)
Proposed half adder	2010	180nm, 3V	1.8ns	76	112 µW(1G Hz)
Proposed full adder	2010	180 nm,3V	2.02ns	148	84µW(250MHz)